REMARKS

This newly cited reference to Dangelo et al. (U.S. Patent No. 5,555,201) is no different than the Dangelo et al. (U.S. Patent No. 6,216,252) recited in the previously Office Actions and which was extensively discussed by Applicant and the Examiner during the in-office interview with Attorney Greeley and Dr. Debashis Bhattacharya on October 15, 2004. During that in-office interview Applicant explained that wherein the present invention is directed to designing, mapping and evaluating a transistor-level representation of the design-specific cell, US Patent No. 6,216,252 (Dangelo et al.) is directed to a **gate-level representation**. In this regard Dangelo '252's gate-level or logic-level deal with cells having Boolean expression capability, i.e., NAND, NOR, etc.). The gate-level or logic-level designs or cells of Dangelo '252 are at a much higher level than the transistor-level design-specific cells according to the present invention. That is, the gate-level or logic-level designs of Dangelo '252 are directed to the "NAND"/"NOR" Boolean gate level cells which by themselves include transistors. However, only the "NAND"/"NOR" Boolean gate level cells themselves may be automatically arranged by the design engineer, whereas the present invention allows the design engineer to now design, map and evaluate at the transistor-level, thereby automatically creating a new design-specific cell which heretofore did not exist. In accordance with Dangelo '252, Applicant clearly demonstrated that it cannot alter the transistor-level in the specific Boolean gate level cells, by optimizing the number of transistors, sizes of transistors, etc. such as that recited in the claims of the present invention.

Similarly, the newly cited Dangelo '201 is no different than the previously cited Dangelo '252 in that it also only relates to gate-level or logic-level cell representations and neither describes nor suggests the transistor level design specific cells recited in the claims of the present invention. Dangelo '201 cannot alter the transistor-level by optimizing the number of transistors, sizes of transistors, etc. such as that recited in the claims of the present invention.

Figure 6 of Dangelo '201 specifically recites that "A Memory Compiler (MemComp) 602 takes the high level specification for memory mega-cells and produces logic and layout files for the purpose of simulation, testing and layout. The objective is to provide the Design Compiler (Optimizer) 604 with an accurate timing description of and drive capability information for the memory block." (Col. 20, lines 43-48). Compiler 604 is clearly identified as a "Gate Level Optimizer" in Figure 6. Col. 20, lines 51-55, further states that "The memory block created by MemComp 602 is provided in the same format as the internal macro-cells, i.e. a net list of **primitive transistors**, which cannot be read directly by the Design Compiler 604." Clearly, Dangelo '201 is dealing solely with gate-level or logic-level design and higher levels rather than transistor-level designs as recited in the present invention. In particular, Dangelo '201 clearly states that is utilizing a "Gate Level Optimizer" and that its net list comprises primitive transistors, rather than the recited design specification of the present invention. That is, the "design specification: is preferably selected from the group consisting of: size (area), signal timing, transistor sizing, number of transistors, power consumption, length of interconnects within said design-specific cell, output signal strength, input signal impedance, noise characteristics, and a combination thereof. The "primitive transistors" recited in the net list according to Dangelo '201 do not pertain go the design specifications recited in the transistor-level cell designs according to the present invention.

The fact that Dangelo '201 pertains only to Gate-Level or Logic-Level cell designs rather than the Transistor-Level cell designs recited in the claims of the present invention can be well understood by reference to Figures 12 (i.e., where the mapping 1120 and optimizer 1124 go to a "Gate-Level Netlist" 1126 before layout, and Figure 33b wherein the lowest level is identified as "Logic Level" 3343.

No where in Dangelo '201 does it describe or suggest the transistor-level

cell design as recited in the claims of the present invention.

The sections of Dangelo '201 specifically identified in the outstanding Office Action as reciting that which is claimed in the present invention, neither describe nor suggest that which is recited in the currently pending claims. In particular, the Office Action refers to Col. 2, lines 35-47 and Col. 4, lines 25-67, as support that Dangelo '201 describes the element of claim 1 pertaining to "receiving a design specification for electrical behavior or transistor level characteristics of said design specific cell." To the contrary, Col. 2, lines 35-47 specifically state that "... A design entity may represent an entire system, a sub-system, a board, a chip, a macro-cell, a logic gate, or any level of abstraction in between. " Clearly, this section of Dangelo '201 identifies the "logic gate" as the lowest level of design. This clearly demonstrates that Dangelo '201 neither describes nor suggest that its mapping pertains to anything lower that "logic gate" level, which specifically excludes the transistor-level recited in the present invention.

Col. 4, lines 25-67, of Dangelo '201 pertains to a discussion regarding prior art simulations and not to the claimed transistor letter cell design recited in the present invention. This referenced section in no way describe or suggests design optimization at the transistor level or the creation of a new cell at the transistor level as recited in claims 1-38.

The outstanding Office Action directs applicant to Col. 29, lines 15-20, for support for its position that the step of "mapping to a transistor-level representation of said design-specific cell, said mapping based on said design specification" neither describes nor suggests this step. To the contrary, this provision of Dangelo '201 pertains solely to "mapping from one level of design representations". This provision of Dangelo '201 in no way describes the mapping to a transistor-level, as no wherein Dangelo '201 does it refer to any level of mapping lower than the Gate-Level, and certainly therein is no

description or suggestion anywhere in Dangelo '201 of mapping to a "transistor-level" as recited in the claims of the present invention. Similarly, Col. 33, lines 33-47, only refers to the fact that "... a schematic diagram can represent a transistor-level circuit diagram of an integrated circuit". Nowhere in that references section of Dangelo '201 does it describe or suggest that the mapping of a transistor-level representation of said design-specific cell, said mapping based on said design specification, as recited in the present invention.

The top-down designs referenced in Col. 50, lines 15-19, recited in the outstanding Office Action as describing the step of "evaluating said transistor-level representation of said design-specific cell for meeting said design specification", neither describes nor suggests any transistor-level design. To the contrary, the Top-Down Design Methodology only list the following milestones, none of which pertain to transistor-level design as recited in the claims of the present invention: (a) architectural definition and design completion, (b) behavior definition and design completion, (c) functional definition and design completion, (d) logic definition and design completion, (e) timing definition and design completion, (f) physical definition and design completion (area, topology, floorplanning routing), (g) power definition, (h) test definition and design completion, and (I) package definition and design completion.

The Office Action recites Col. 2, lines 25-35 as reciting that which is recited in claim 2, which recites, inter alia, "said step of evaluating comprises evaluating said transistor-level representation of said design-specific cell based on a specific design context in which said design-specific cell is to be used." The only thing in common between claim 2 and that which is described in Col. 2, lines 25-35, is the term "context". Other than that common term there is no description in this section of Dangelo '201 which describes or suggests anything remotely pertaining to that which is recited in claim 2 of the present invention.

Claim 3 recites, inter alia, that the step of receiving comprises receiving a

description of the design-specific cell. The outstanding Office Action refers to Col. 1, lines 58-67, as describing that which is recited in claim 3. Applicant has thoroughly reviewed Col. 1, lines 58-67, and cannot find any description or suggestion of a step of receiving a description of the design-specific cell.

Claim 4 recites, inter alia, that the description is selected from a group consisting of a netlist representation, a descriptive language representation, and a standard-cell representation of said design-specific cell, wherein said standard-cell is used in an IC design process. Other than the term "netlist", Applicant cannot find any description or suggestion of that which is recited in Claim 4 in Col. 21, lines 10-15, of Dangelo '201, as recited by the outstanding Office Action as teaching the method of Claim 4. The recitation of the term "netlist" neither describes nor suggests that which is recited in claim 4 or any of the claims in the present invention. Moreover, the outstanding Office Action refers to Figure 1 of Dangelo '201 to depict, in isolation, a standard-cell representation". A thorough review of Figure 1 and the corresponding description thereof on Col. 17, lines 21-67, neither describes nor suggests that which is recited in either Claim 4 or the isolated phrase "a standard-cell representation."

Similar to the previously cited Dangelo '252 patent, Dangelo '201 relates to "NAND"/"NOR" Boolean **gate level cells** and neither describes nor suggests that which is recited in the claims of the present invention, e.g., a method of designing, mapping and evaluating a new design-specific cell at the **transistor-level**. This unique method of the present invention allows the design engineer to automatically optimize the size (area), signal timing, transistor sizing, number of transistors, power consumption, fault tolerance, integrity characteristics, noise characteristics, and a combination thereof at the transistor-level, which was heretofore not capable with the "NAND"/"NOR" Boolean gate level cells design and implementation system disclosed in either Dangelo '252 or '201. That is, Dangelo '201 neither describes nor suggests that which is recited in the present invention of creating a unique design-specific cell at the transistor-level. Rather,

Dangelo '201 utilizes pre-existing "NAND"/"NOR" Boolean gate level cells found in a standard cell library to create a system or circuit, but has no capability to create a completely new design-specific cell at the transistor-level that was not previously found in the standard cell library or to optimize the circuit at the transistor-level.

In summary, it is respectfully submitted for the reasons set forth above, that this amendment places the application in condition for allowance. Accordingly, it is respectfully requested that claims 1-38 be allowed and the application be passed to issue.

Respectfully Submitted,

Date: 3-28-05

Paul D. Greeley, Esq.
Reg. No. 31,019
Attorney for Applicant(s)
Ohlandt, Greeley, Ruggiero & Perle, L.L.P.
One Landmark Square, 10th Floor
Stamford, CT 06901-2682
(203) 327-4500